Choosing a sample-and-hold amplifier is not as simple as it used to be

Sample-and-hold modules, which are particularly useful in high-speed data acquisition systems, are now available in unprecedented variety; a grasp of how they work makes it easier to pick the right one for a given job

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☐ As a naturally analog world goes steadily digital, the sample-and-hold amplifiers that often accompany analog-to-digital converters also increase in variety. The modules now available range from general-purpose units to high-speed, high-accuracy versions and cost anywhere from $40 to $400. Unless their characteristics are understood, it's no longer simple to select the right sample-and-hold for a given application.

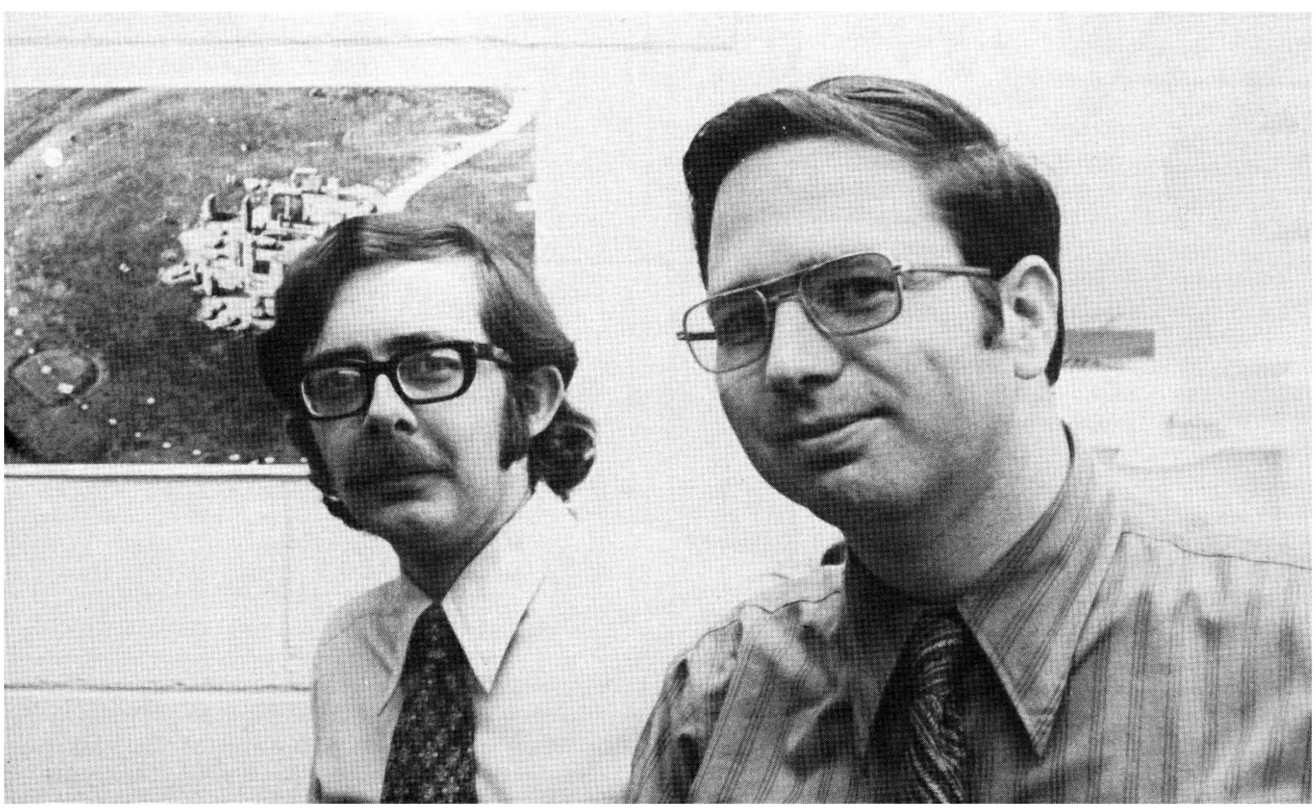
Functionally, every sample-and-hold amplifier tracks an analog signal and, when directed by an external digital command, freezes its output at the instantaneous value of the input. But the individual parameters of this performance vary in importance with the particular application.

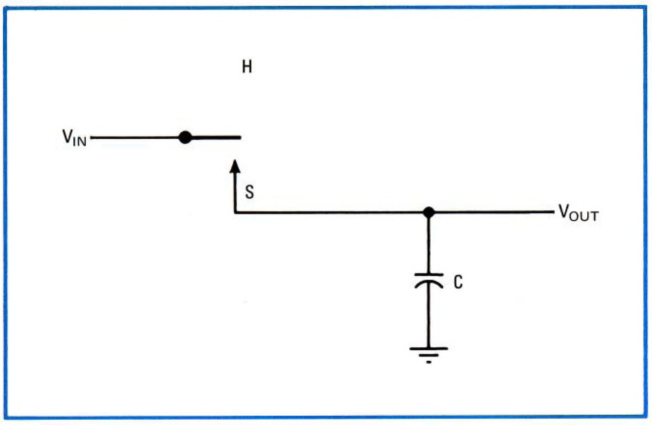
And the applications are numerous. Sample-and-hold amplifiers are particularly useful where fast-changing signals must be multiplexed in data acquisition systems or where momentary signals must be captured and held. They are frequently used in sampled-data systems to decrease system aperture time with a-d converters, and in display systems to provide smooth, glitch-free outputs from d-a converters. Other applications include pulse stretching, data distribution to multiple readouts, peak and valley following, and ratio-measurement of time-averaged variables.

The basic circuits

Probably the simplest form of sample-and-hold amplifier is the capacitor-switch combination shown in Fig. 1. With this circuit, the hold command is given when the switch is thrown from position S to position H. But though the circuit works effectively with very slowly

Experience. Authors Walter Patstone (foreground) and Craig S. Dunbar have been working together at Teledyne Philbrick for the past four years on the application of circuit modules. One result of their study of applications problems is the model 4853 sample-and-hold amplifier.





pacitor and a switch make an effective sample-and-hold circuit.

changing signals, it causes too much source and output loading to be of much practical use.

Most practical modular sample-and-holds are designed for noninverting unity-gain operation, but important new inverting designs are now available. In both types, the control inputs are normally operated at standard logic levels and are usually TTL-compatible. Typically logic 1 is the sample command and logic 0 is the hold command.

The basic noninverting sample-and-hold amplifier consists of a resistor, a switch, a capacitor, and an op amp (Fig. 2a). When the switch is closed, the capacitor charges (or discharges) exponentially to the input voltage just as in the simple capacitor example. The output of the operational amplifier follows the capacitor voltage precisely. Again, when the switch is opened, the capacitor holds the instantaneous value of the input voltage. The advantage of the op-amp follower in this circuit is that, once the charge is acquired and the switch is opened, output loading will not discharge the capacitor.

In such a circuit, a FET switch would most probably be used, and the op amp would have a FET input. However, the storage capacitor still loads the input sources, and this loading, if R is too low, may make the source oscillate or overload it. When the source is overloaded at acquisition time, recovery time normally is long.

Increasing R to prevent these problems will slow the response time, and instead, a buffer amplifier can be added in front of the capacitor (Fig. 2b). Here the input is isolated from the holding capacitor, and the buffer amplifier provides the capacitor charging current.

This circuit is pretty fast, but since the amplifiers work independently, a summation of errors results. Consequently, if low-frequency tracking accuracy is more important than speed, the feedback loop can be closed around both amplifiers, forcing both to track as one amplifier (Fig. 2c).

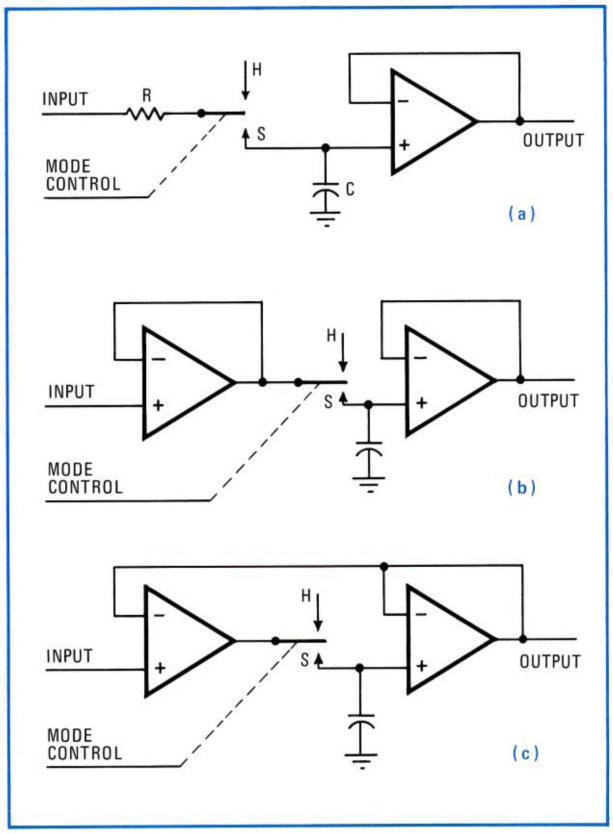
The other basic type of sample-and-hold amplifier—the inverting, or integrating, circuit—is shown in Fig. 3. Because the capacitor is in the feedback loop, the input is isolated, and the FET switch operates at ground potential, minimizing leakage current and switching time, while the amplifier is not bothered by a common-mode signal. Although this type of circuit does not require a buffer amplifier to charge the capacitor or isolate the input, its input impedance is significantly lower than in the buffered noninverting types. Therefore, the signal source must have a reasonable drive capability and a low output impedance. No problem will arise, however, if an op amp is used as a preamp.

The modification of the inverting sample-and-hold amplifier shown in Fig. 3b places an inverting buffer amplifier in front of the switch but within the feedback loop. Since the inverting input is floating, high-input impedance is provided. If a FET buffer is used, the current required to drive the circuit will be in the picoampere range. However, the addition of the input buffer introduces common-mode error, and additional nonlinearity error, besides reducing speed.

The parameters

In selecting the proper sample-and-hold for a given application, certain specifications are more critical than others. The nomenclature for these is not yet standardized, but the following discussion is based on terms generally accepted in the industry.

Aperture time is the apparent time elapsed between the hold command and the effective opening of the hold switch (Fig. 4a). As the diagram shows, the error caused by the aperture time increases both with the aperture time itself and with the rate of change of the input signal. In actual practice, properly designed FET switching circuits can keep the aperture time, or turn-off time, down to a few nanoseconds.



switch circuit's sensitivity to output loading. Source loading, however, remains a problem unless an input buffer amplifier is added (b). Putting a feedback loop around both amplifiers improves low-frequency performance but slows the system (c).

Aperture time, by itself, is not a problem for most applications; it may be regarded as a timing delay. Therefore, to the extent that it is repeatable, it may be compensated for by advancing the control timing. Typical values of aperture time for high-performance sample-and-hold range from 5 to 40 nanoseconds.

Aperture-time uncertainty is the term for the repeatability of the aperture time. It can also be thought of as the uncertainty in the sample-to-hold transition time, or the difference between the maximum and the minimum aperture times experienced with a particular amplifier. This parameter is a major factor in determining the maximum signal frequency which can be accurately sampled. Commercially available sample-and-hold amplifiers with maximum aperture uncertainty times of ±1 nanosecond will permit the sampling of 16-kilohertz signals to a 12-bit (.01%) accuracy.

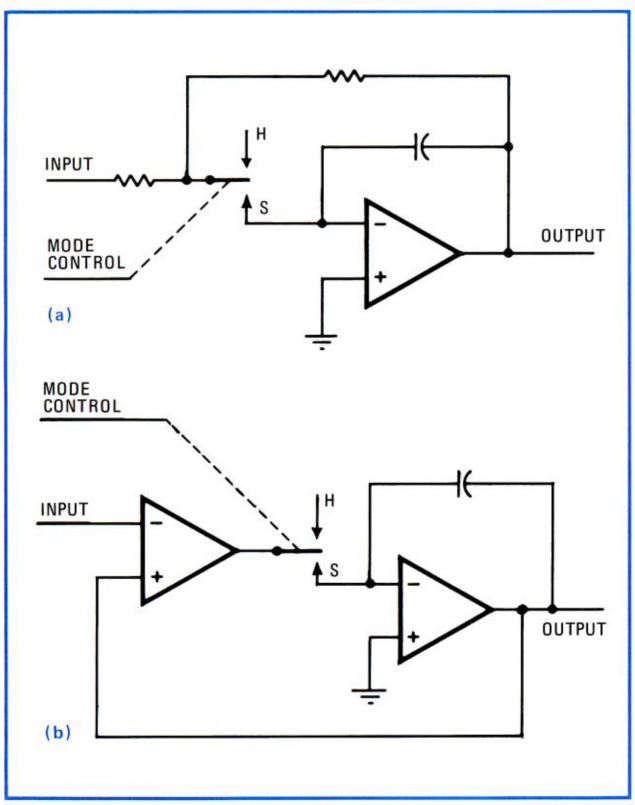
In digitizing a continuously varying audio or video signal the aperture uncertainty time must be low to minimize jitter and the noise it causes on the reconstructed signal. Note, too, that in this application the delay identified with aperture time is usually unimportant, and no delay compensation is necessary.

Acquisition time is the length of time that elapses between the sample command and the precise instant at which the output voltage is tracking the input voltage to within a specified accuracy (Fig. 4b). For the switch-capacitor circuit, acquisition time depends on the charging current available from the driving source current. When the switch is closed, the capacitor charges or discharges exponentially with a time constant that is a function of the source impedance and hold capacitance.

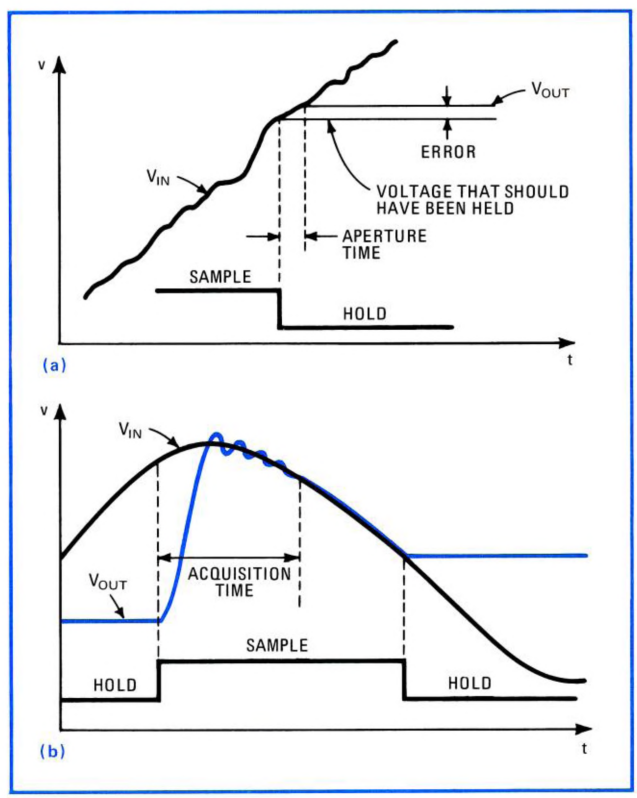
The worst-case acquisition time occurs when the sample-and-hold circuit must change full scale. Therefore, specifications are normally written in terms of a full-scale voltage step, and the specified accuracy is usually stated as a fraction of a percent of full scale, for example 0.01% or 0.1%. Acquisition time in simple circuits consists primarily of time constants; in more sophisticated designs, amplifier slew rate and settling time have to be included.

One problem that occurs even in the simplest sample-and-circuit hold is the presence of voltage spikes associated with switching transients. These spikes are not only annoying in themselves but also constitute a major source of circuit error. When the capacitor is switched from sample to hold, some charge is transferred to the holding capacitor due to the inter-electrode capacitance of the switch. This charge, translated into an error voltage, is called the *hold jump voltage* by some manufacturers and the *sample-to-hold offset* by others. In packaged circuits, it's usually possible to trim out the jump voltage, but necessary to live with the spikes.

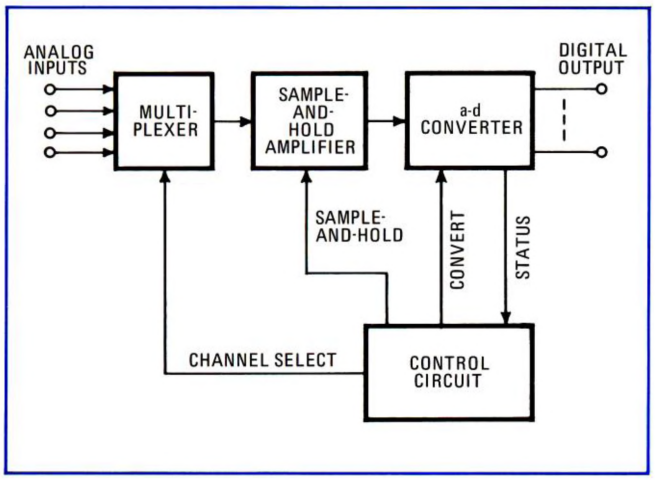
Related specifications are the *sample offset voltage* (the error voltage encountered in the sample mode, which is basically due to the offset voltage of the internal op amp) and the *hold offset voltage* (the error voltage encountered in the hold mode and composed of the



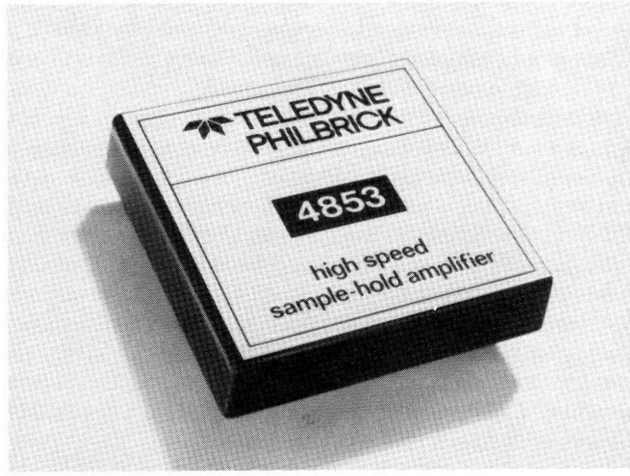
3. Inverting circuit. When a capacitor is inserted in the feedback loop, the inverter effectively isolates the input and minimizes the switching time (a). This approach is used in Teledyne Philbrick's 4853 sample-and-hold amplifier. Input impedance is low, however, unless an input buffer amplifier is added (b).



4. Definitions. Aperture time is the delay between the arrival of the hold command and the actual opening of the switch (a). Acquisition time is the length of time that will elapse before the amplifier starts tracking the input signal to within some specified accuracy after it has been commanded to do so (b).



5. Working within the system. By providing a constant input voltage to the a-d converter while the multiplexer is switching channels, the sample-and-hold circuit eases the converter's speed constraints.



6. Fast and accurate. Philbrick's 4853 is suitable for use with 12-bit converters at speeds up to 20 kHz. Input voltage range is ±10 V, input impedance is 2 kΩ, and aperture time uncertainty is ±1 ns.

hold jump voltage and the sample offset voltage). These three voltages are not major sources of error in most applications because all are trimmable to zero. For driving an a-d converter, it is normally sufficient to trim only the hold offset to zero.

During hold, a small part of the input signal feeds through the capacitance of the switch to the output. This *feedthrough,* which is usually a function of the level and frequency of the input signal, can be thought of as the input-output transfer function of the sample-hold amplifier while in the hold mode. Ideally, feedthrough should be zero.

If a data acquisition system contained an ideal sample-and-hold amplifier, the basic limitation on its throughput (or rate of transmission of data) would be the conversion speed of its a-d converter, because the multiplexer could be switching to another channel during the conversion. However, many commercially available sample-and-hold amplifiers demonstrate such high feedthrough that switching the multiplexer during the conversion period would give rise to intolerable errors. Some modules therefore use a clamping network to limit feedthrough to ±1 millivolt maximum for a ±20-v input step. This permits increased throughput for 12-bit data acquisition systems.

Decay rate

Also while in the hold mode, a typical sample-and-hold amplifier will exhibit a decay of its output voltage over a period of time. This relatively constant output drift, termed the *decay rate,* is usually specified in microvolts per second. For the simple switch-capacitor circuit, it is caused by leakage currents through both the switch and the hold capacitor. In more complex circuits, it should be noted that the decay can be either positive or negative, depending on the polarity of the buffer amplifier bias current. Further, it is usually sensitive to temperature—with FET buffers, at any rate, the bias current doubles for each 10°C rise in ambient temperature.

The importance of the decay rate depends on the length of the hold time and the desired accuracy. In high-speed applications the hold periods are seldom longer than 100 microseconds, so decay rate errors are unimportant even when the decay rate is as high as 1 microvolt per microsecond.

Perhaps the most difficult and sophisticated application for a sample-and-hold amplifier is in a very-high-speed data acquisition system, like the one outlined by the simplified block diagram of Fig. 5. The sample-and-hold circuitry maintains a constant input to the a-d converter during the conversion period while the multiplexer is seeking the next channel to be converted. After the first conversion is complete the sample-and-hold amplifier samples the next input, and the cycle is repeated. Sampling can be synchronized with the other system components, or it can be performed asynchronously.

In such a system, nearly all parameters are important except decay rate—that is, acquisition time, aperture time, aperture uncertainty time, bandwidth and feedthrough must all be considered in the designer's error budget because they all can affect the throughput data rate. The feedthrough is especially critical in multiplexed systems.

Note that the designer of a data acquisition system frequently has a choice of approaches for handling a known throughput rate. For example, many applications allow the use of a sample-and-hold amplifier with a moderate-speed a-d converter as an alternative to a very-high-speed a-d converter. Use of the moderate-speed combination often results in significant cost savings.

In the fast system, decay rate is not very important because the signal is usually not held for any significant length of time. The opposite is true of slow applications, where the most important parameter would be decay rate and all others would be of minor consequence.

One example of such a slow application is the mechanical test system measuring deformation in a titanium aircraft forging that is being subjected to a constantly increasing load. At predetermined points in time the sample-and-hold freezes the transducer signal so that it can be read out and displayed. Here the decay rate should be low enough to keep the reading within the desired accuracy right to the end of the maximum hold period. □